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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,106	08/23/2001	James M. Derderian	4832US (01-0104)	1038

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 11/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding..

D.S

Office Action Summary	Application No. 09/938,106	Applicant(s) DERDERIAN, JAMES M.
	Examiner Junghwa M. Im	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) *1-22,36-39,52 and 65-69* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-35,40-51 and 53-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *03 January 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 23-35, 40-51 and 53-64 in Paper No. 7 is acknowledged.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 25-28, 47 and 48 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding the limitation over coating the discrete elements, the elected embodiment does not show coated wires, rather bare wires are buried in the adhesive layer, for example as shown in Fig. 17 (a completed device).

Pending claims 27 and 48 also recite that a formation of a dielectric layer on the back of the second device, while the corresponding independent claim recites that the second device is positioned "on" the discrete elements. For example, Claim 27 indicates that a dielectric layer is formed between the second device and the discrete elements, then, the second device can not be positioned "on" the discrete elements as recited in Claim 23.

Or is the "second semiconductor device" both the chip and the dielectric layer? If so, claim23 could be understood as describing Fig. 14, for example, which shows contact between wire 38a and dielectric layer 33. But then claim 27 would require an additional dielectric layer, which is not taught. So it would appear that no disclosed embodiment would correspond to claim 27 (or claim 48), because no embodiment discloses both a dielectric layer and contact between discrete conductive element and a backside of a semiconductor device.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 27 and 48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As noted above, it is not clear what is meant by a "semiconductor device". There does not appear to be any way to correlate the claim language of claim 27 and 48 to the disclosure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 23-35, 40-51 and 53-64 are rejected under 35 U.S.C. 103(a) as being unpatentable under obviousness over Lee et al. (U.S. Pat. No. 6,388,313).

Regarding claim 23, Lee et al. show a device in Figure 1 to use a method for assembling semiconductor devices, comprising;

providing a first semiconductor device 21 ;

placing discrete conductive elements 22 over portions of said first semiconductor device; and

positioning a second semiconductor device 23,24 at least partially over said first semiconductor device (col.6, lines 13-14) and contacting at least some of said discrete conductive element with a back side of said semiconductor device (see also Fig. 3).

Also see the respected portions of the specification such as for first embodiment.

Regarding claim 24, Lee et al. show a method, wherein

the positioning the second semiconductor device comprises positioning the second semiconductor device on said at least some of discrete conductive elements with the back side and the discrete conductive elements in mutual electrical isolation (col. 5, lines 40-44).

Regarding claim 25, Lee et al. show a method comprising: providing a dielectric coating on at least portions of the discrete conductive elements (col. 5, lines 40-44).

Regarding claim 26, Lee et al. show a method wherein the providing comprises forming at least one of a dielectric oxide and a dielectric polymer coating on at least said portions of the discrete conductive elements (col. 5, lines 22-24).

Regarding claim 27, with understanding that a dielectric layer formed between the

top surface of the first device and the back surface of the second device, Lee et al. show a forming a dielectric layer 23 in Fig. 1 at least portions of the back side.

Regarding claim 28, with understanding that a dielectric layer formed between the top surface of the first device and the back surface of the second device, Lee et al. show the forming is effected prior to the positioning the second semiconductor device

Regarding claim 29, Lee et al. show applying a quantity of adhesive material to at least an active surface of the first semiconductor device (col. 5, lines 24-25).

Regarding claim 30, it is obvious that the device of Lee et al. show drawing the second semiconductor device toward the first semiconductor device after applying the adhesive on the first device.

Regarding claim 31, Lee et al. show the drawing is effected by at least one of capillary action of the adhesive material, curing of the adhesive material, application of heat to the adhesive material, and vibration of the adhesive material (col. 5, lines 32-40).

Claims 32-34 have been discussed previously.

Regarding claim 35, Lee et al. show the drawing is effected during curing of the adhesive material (col. 5, lines 32-41).

Regarding claim 40, Lee et al. show securing the first semiconductor device and a substrate to one another (col. 5, lines 5-6).

Regarding claim 41, Lee et al. show wherein the placing the discrete conductive elements comprises securing the discrete conductive elements to contact areas of the substrate and the bond pads of the first semiconductor device (col. 5, lines 8-10).

Regarding claim 42, Lee et al. show the securing comprises electrically

connecting bond pads of the second semiconductor device to the corresponding contacts areas of the substrate (col. 5, lines 13-16).

Regarding claim 43, Lee et al. show encapsulating at least portion of at least one of the substrate, the first semiconductor device, and the second semiconductor device (col. 6, lines 32-36).

Regarding claim 44, Lee et al. show forming external conductive elements 27 in Fig. 1 on the substrate in electrical communication with corresponding contact areas (col. 5, lines 1-4).

Regarding claim 45, Lee et al. show a device in Figure 4 to use a method for assembling semiconductor devices in stacked arrangement with the stacked arrangement having a height substantially equal to combined thicknesses of each of the semiconductor devices and distances discrete conductive elements 22, 25 associated therewith protrude above each semiconductor device (col. 5, lines 44-48), comprising:

providing a first semiconductor device 21 with discrete conductive elements 220 protruding from an active surface thereof; and

providing a second semiconductor device 23 at least partially over the first semiconductor device (col. 6, lines 12-15) and on at least some of the discrete conductive elements.

Claims 46-51 and 53-55 has been discussed previously.

Regarding claim 56, Lee et al. show biasing at least one of the first and second semiconductor devices toward the other of the first and second semiconductor devices (col. 4, lines 54-68).

Regarding claim 57, Lee et al. show controlling the biasing by means of adhesive

(col. 4, lines 54-68).

Regarding claim 58, Lee et al. show the controlling the biasing comprises controlling the biasing force to a level sufficient to deform, kink, bend, or collapse the discrete conductive elements.

See the respective portions of the specification such as col. 5, lines 24-32.

Claim 59 has been discussed previously.

Regarding claim 60, Lee et al. show connecting the discrete conductive elements to corresponding contact areas of the substrate (col. 5, lines 8-10).

Regarding claim 61, Lee et al. show establishing electrical communication between bond pads of the second semiconductor device and the corresponding contact areas of the substrate (col. 6, lines 8-12).

Regarding claim 62, Lee et al. show establishing communication comprises placing additional discrete conductive elements 25 in Fig. 1 between each of the bond pads and the corresponding contact area of the corresponding contact areas.

Claims 63 and 64 have been discussed previously.

Claim Rejections - 35 USC § 103

Claims 23 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable under obviousness over Foster (U.S. Pat. No.6,437,449).

Regarding claim 23, Foster shows a device in Figure 2 to use a method for assembling semiconductor devices, comprising;

providing a first semiconductor device 108 and 115 ;

placing discrete conductive elements 116, 122 and 124 over portions of said first semiconductor device; and

positioning a second semiconductor device 140 and 146 at least partially over said first semiconductor device and contacting at least some of said discrete conductive element with a back side of said semiconductor device

Regarding claim 45, Foster show a device in Figure 2 to use a method for assembling semiconductor devices in stacked arrangement with the stacked arrangement having a height substantially equal to combined thicknesses of each of the semiconductor devices and distances discrete conductive elements associated therewith protrude above each semiconductor device, comprising:

providing a first semiconductor device 108 and 114 with discrete conductive elements 116, 122 and 124 protruding from an active surface thereof; and

providing a second semiconductor device 140 and 146 at least partially over the first semiconductor device and on at least some of the discrete conductive elements.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (703) 305-3998. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for

the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JMI
November 18, 2002

Sara W Crane

Sara Crane
Primary Examiner